In the Claims:

1. (Currently Amended) An apparatus, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address

storage locations, the command sequencer and serializer unit to control a data cache

~~associated with~~ located on a memory module, the command sequencer and serializer unit

to reduce a first plurality of address and command signals down to a more narrow set of

signal lines coupled to the memory module, the more narrow set of signal lines forming a

point-to-point interconnect between the command sequencer and serializer unit and the

memory module.

2. (Original) The apparatus of claim 1, further comprising:

a plurality of arrays of tag address storage locations, each of the plurality of arrays

of tag address storage locations corresponding to one of a plurality of memory modules.

3. (Original) The apparatus of claim 2, each of the plurality of arrays of tag

address storage locations organized into a plurality of ways.

4. (Original) The apparatus of claim 3, each of the plurality of arrays of tag

address storage locations organized into 4 ways.

5. (Currently Amended) The apparatus of claim 1, the ~~command sequencer and~~

~~serializer unit to control a data cache associated with a memory module by delivering~~

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~~commands over~~ <u>more narrow set of signal lines including</u> a plurality of command and address lines.

6. Cancelled

7. (Currently Amended) ~~An apparatus~~ <u>A memory module</u>, comprising:

a memory device; and

a data cache coupled to the memory device, the data cache controlled by commands delivered by a memory controller component over a memory bus, the memory controller component including an array of tag address storage locations<u>, the memory controller component not located on the memory module</u>.

8. (Currently Amended) The ~~apparatus~~ <u>memory module</u> of claim 7, further comprising a command decoder and deserializer unit to receive command and address information from the memory controller component, the command decoder and deserializer unit providing control for the data cache.

9. (Currently Amended) The ~~apparatus~~ <u>memory module</u> of claim 8, wherein the data cache is organized into four ways.

10. (Currently Amended) A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

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an array of tag address storage locations, and

a command sequencer and serializer unit coupled to the array of tag

address storage locations; and

a memory module separate from and coupled to the memory controller via a

memory bus, the memory module including

a memory device, and

a data cache coupled to the memory device, the data cache controlled by

commands delivered by the memory controller.

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11. (Currently Amended) The system of claim 10, the memory bus including a

point-to-point interconnect to couple the memory controller to the memory module.

12. (Original) The system of claim 10, the memory controller further including a

plurality of arrays of tag address storage locations.

13. (Original) The system of claim 12, further comprising a plurality of memory

modules, each of the plurality of memory modules including at least one of a plurality of

memory devices and one of a plurality of data caches, each of the data caches controlled

by commands delivered by the memory controller.

14. (Original) The system of claim 13, the plurality of arrays of tag address

storage locations and the plurality of data caches organized into four ways.

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15. (Currently Amended) A method, comprising:

receiving a read request at a memory controller;

performing a tag look-up within the memory controller to determine whether there

is a cache hit for the read request; and

fetching a line of cache data from a data cache located on a memory module if the

tag look-up indicates a cache hit, the memory module separate from the memory

controller and coupled to the memory controller via a memory bus.

16. (Original) The method of claim 15, further comprising:

loading a line of data from a memory device located on the memory module to the

data cache if the tag look-up indicates a cache miss; and

delivering the line of data to the memory controller.

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